NASA TECH BRIEF

NASA Pasadena Office



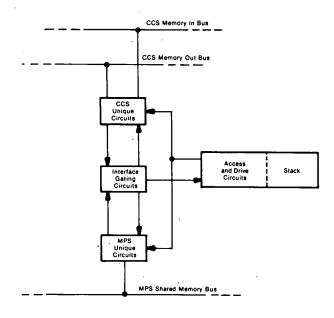
NASA Tech Briefs announce new technology derived from the U.S. space program. They are issued to encourage commercial application. Tech Briefs are available on a subscription basis from the National Technical Information Service, Springfield, Virginia 22151. Requests for individual copies or questions relating to the Tech Brief program may be directed to the Technology Utilization Office, NASA, Code KT, Washington, D.C. 20546.

High-Speed Fault-Tolerant Telemetry/Computer Interface

A fault-tolerant telemetry/computer interface has been developed which allows memory sharing by two data processing systems and maintains the integrity of the fault-tolerant environment of the computer. In this case, the interface is designed for a measurement processing system (MPS) and a central computer and sequencer (CCS). This is made possible by providing each side with its own data register and address register and by using a common timing source. Although both of these systems are used on spacecraft, a similar approach is suitable for ground applications.

Basically the MPS is a programable system which requires direct access to a read-write memory. It stores programs in the memory and provides a buffer memory for spacecraft system parameter values. These values are processed for transmission to Earth. The CCS, on the other hand, uses spacecraft system parameters to monitor and evaluate the systems.

As shown in the illustration, each shared memory includes interface gating circuits and MPS unique circuits which are added to the original CCS read-write memory. The interface gating circuits provide OR functions for the signals feeding from both the CCS and the MPS unique circuits. Both the MPS and the CCS can access memory at their maximum accessing rates without interfering with each other. The assignment of memory modules is controlled by the CCS. In addition, whatever memory modules are turned on for use by the CCS for its own programs, another memory module is turned on and assigned to the MPS as a shared memory.



Shared Memory Block Diagram

Note:

Requests for further information may be directed to:

Technology Utilization Officer NASA Pasadena Office 4800 Oak Grove Drive Pasadena, California 91103 Reference: TSP74-10296

(continued overleaf)

Patent status:

This invention is owned by NASA, and a patent application has been filed. Inquiries concerning non-exclusive or exclusive license for its commercial development should be addressed to:

Patent Counsel
NASA Pasadena Office
4800 Oak Grove Drive
Pasadena, California 91103

Source: George C. Gilley of Caltech/JPL under contract to NASA Pasadena Office (NPO-13139)